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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,345	06/28/2001	Krishnamurthy Soumyanath	42390.P11206	8325

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Seth Z. Kalson
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER

NGUYEN, HAI L

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 08/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/896,345	SOUMYANATH ET AL.
	Examiner Hai L. Nguyen	Art Unit 2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 16 July 2002.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 2-6 and 8-12 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 2-6 and 8-12 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 24 September 2001 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.
 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.
 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) The translation of the foreign language provisional application has been received.
 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____.
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 	6) <input type="checkbox"/> Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's response letter received on 07/16/02 has been reviewed and considered with the following results:

As to the prior art rejections to claims 1-12, the arguments and/or comments by the applicant have been carefully reviewed, but are not persuasive. The response to applicant's arguments is addressed as set forth below.

A new action on the merits appears below in view of applicant's amendments to the claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 2, 4, 8, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Sudo et al. (US 5,812,018; previously cited).

With regard to claims 2 and 4, Sudo et al. discloses in Fig.1 a circuit, and a method of use thereof, comprising an input port (N10) having an input signal voltage (VBB); an output port (15) having an output voltage (VPP); and a field-effect-transistor (M11) having a gate, a first terminal, and a second terminal; wherein the gate and the first terminal are each connected to the input port, and the second terminal is connected to the output port, the output voltage is

inherently indicative of a local time-average maximum of the input signal voltage, and wherein in steady state the FET is coupled to operate in a sub-threshold region if the input signal voltage is stationary.

With regard to claims 8 and 10, Sudo et al. discloses in Fig.1 a circuit, and a method of use thereof, comprising an input port (N15) having an input signal voltage (VPP); an output port (10) having an output voltage (VBB); and a field-effect-transistor (M15) having a gate, a first terminal, and a second terminal; wherein the first terminal is connected to the input port, and the gate and the second terminal are each connected to the output port, the output voltage is inherently indicative of a local time-average minimum of the input signal voltage, and wherein in steady state the FET is coupled to operate in a sub-threshold region if the input signal voltage is stationary.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3, 5, 9, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sudo et al.

With regard to claims 3 and 5, the above discussed circuit of Sudo et al. meets all of the claimed limitations except for the limitation that the FET has a device width, wherein the FET has a leakage current in excess of 1 micro ampere per micron of device width. It would have

been obvious to one of ordinary skill in the art at the time of applicant's invention was made to set the leakage current for meeting specific condition which is in each case optimally matched to its application. Since it has been held that discovering an optimum skill in the art. See *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 9 and 11 are similarly rejected, note the above discussion with regard to claims 3 and 5.

6. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, Figs.1-4 in the present application, in view of Nakano (US 5,917,366; previously cited).

With regard to claims 6 and 12, the prior art in Figs.1-4 shows a circuit to provide direct current (DC) offset correction to an input signal voltage, the circuit comprising an input port (IN in instant Fig.4) having the input signal voltage; a field-effect-transistor (402) which can be replaced by a diode (202 in Fig.2); and a DC offset correction unit (406) responsive to the DC offset correction voltage to subtract the DC offset correction voltage from the input signal voltage. Figs.1-4 of the prior art meets all the claimed limitations, except for a field-effect-transistor (702 in instant Fig.7) connected as recited in the claim. Nakano teaches in Figs.2-7 a circuit having field-effect-transistors (Q11-Q14) that are substituted for diodes. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize that teaching of Nakano in the prior art (Figs.1-4) for the advantage of being able to reduce the threshold voltage of the field-effect-transistor. Also, it would have been obvious to one of ordinary skill in the art to connect the gate to either input or output which is in each case optimally matched to its application, i.e., direct the current to flow in a desired

direction. Furthermore, the new added limitation is also met by the prior arts, note the above discussion with regard to claims 3 and 5.

Response to Arguments

7. Applicant's first argument is that "Nowhere does Sudo teach a circuit having an output voltage that is indicative of a local time-average maximum", has been considered but is not persuasive. Even though Sudo does not disclose that result, such as "so that the output voltage is indicative of a local time-average maximum of the input signal voltage". Since all of the structural limitations in the claims are clearly anticipated by the reference, inherently, that result function will also be met.

Applicant's next argument is that "in Fig. 1 of Sudo, the output port VPP is not connected to a terminal of transistor M11. Instead, there are several transistors connected between output port VPP and transistor M11 with gates clocked by clock signals", has been considered but is not persuasive because "connected" should be understood as there is one/or some intermediate element(s) being connected between the output port VPP and transistor M11. Therefore, that claimed limitation is clearly anticipated by the reference.

Applicant's last argument is that "The circuit of Sudo is not relevant to the present invention. There simply is no motivation, upon reading Sudo, to practice the claimed invention for which the FET operates in its sub-threshold region when in steady state and when the input signal voltage is stationary", has been considered but is not persuasive. Even though Sudo does not disclose that limitation, such as "the FET is coupled to operate in a sub-threshold region if the input signal voltage is stationary". Since the input signal voltage is stationary and all of the

structural limitations in the claims are clearly anticipated by the reference, inherently, that recited function will also be met. The rejections of record are still believed to be proper and are therefore maintained as set forth above.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 703-306-9178 and Right Fax number is 703-746-3951. The examiner can normally be reached on Monday-Thursday.

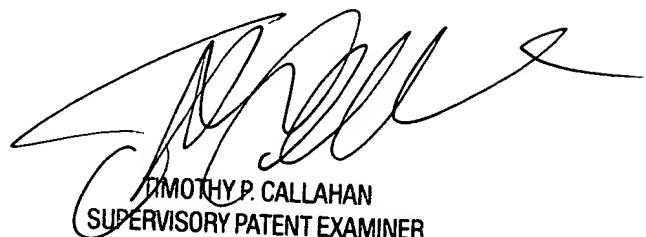
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the

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organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HAI L. NGUYEN
August 19, 2002



TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800